

In the claims:

For the Examiner's convenience all pending claims are presented herein.

No claims have been amended:

- 1 1. A system to test a bus, the system comprising:
2 at least one instruction memory to store a predefined bus stimuli
3 instruction, the predefined bus stimuli instruction representing a
4 bus transaction; and
5 at least one phase generator coupled between the bus and the instruction
6 memory, the at least one phase generator to provide signals to the
7 bus corresponding to the bus transaction in response to the
8 predefined bus stimuli instruction.
- 1 2. The system of claim 1, wherein the instruction memory stores a plurality
2 of predefined bus stimuli instructions, the predefined bus stimuli
3 instructions representing bus transactions.
- 1 3. The system of claim 1, wherein the instruction comprises an instruction
2 word having a predefined length.
- 1 4. The system of claim 1, wherein the at least one phase generator is further
2 responsive to signals received from the bus.
- 1 5. The system of claim 2, further comprising a response memory coupled to
2 the phase generator storing predefined responses to signals received from
3 the bus.

- 1 6. The system of claim 1, wherein the at least one phase generator includes at
2 least one digital logic device responsive to the instructions and at least one
3 phase engine for controlling timing of the bus stimuli.
- 1 7. The system of claim 6, wherein the digital logic device comprises a field
2 programmable gate array.
- 1 8. The system of claim 6, wherein the digital logic device comprises an
2 application specific integrated circuit.
- 1 9. The system of claim 6, wherein the at least one digital logic device
2 includes a control portion for providing bus control signals and a data
3 portion for sending data to the bus.
- 1 10. The system of claim 9, wherein the control portion includes a flow logic
2 device, a request logic device, and a data logic device.
- 1 11. The system of claim 6, wherein the at least one phase engine includes at
2 least one logic level translation device.
- 1 12. The system of claim 6, wherein the at least one phase engine comprises a
2 system phase engine, an arbitration phase engine, a request phase engine, a
3 snoop/error phase engine, and a data phase engine.
- 1 13. The system of claim 9, further comprising a data memory coupled to the
2 data portion.
- 1 14. The system of claim 9, wherein the data portion further receives data from
2 the bus.

1 15. A system to test a bus, the system comprising:
2 an instruction memory storing digital data representing a predefined
3 sequence of bus stimuli;
4 a flow logic device responsive to the instruction memory;
5 a request logic device responsive to the instruction memory;
6 a data logic device responsive to the instruction memory;
7 a data memory coupled to the data logic device storing data to be
8 exchanged with agents on the bus;
9 a system protocol generator coupled to the bus and the flow logic device;
10 an arbitration protocol generator coupled to the flow logic device and the
11 bus;
12 a request protocol generator coupled to the flow logic device, the request
13 logic device and the bus;
14 a snoop/error protocol generator coupled to the request logic device and
15 the bus;
16 a data protocol engine coupled to the data logic device; and
17 a transaction response memory coupled to the flow logic device and the
18 request logic device storing digital data representing predefined
19 responses to signals received from the bus.

1 16. A system to test a bus, the system comprising:
2 a first means for storing instructions representing predefined bus stimuli;
3 and
4 second means for providing signals to the bus in response to the stored
5 instructions.

- 1 17. The system of claim 16, further comprising third means for storing data
2 representing predefined responses to signals received from the bus, and
3 wherein the second means implements the predefined responses based on
4 the signals received from the bus.
- 1 18. The system of claim 16, further comprising fourth means for controlling
2 the timing of the signals provided to the bus by the second means.
- 1 19. The system of claim 16, further comprising fifth means for storing data to
2 be exchanged with agents on the bus, wherein the second means transmits
3 data from the fifth means in response to the instructions stored in the first
4 means.
- 1 20. The system of claim 19, wherein the second means further receives data
2 from the bus and stores the data in the fifth means.
- 1 21. A method for testing a bus comprising:
2 receiving instruction words representing predefined bus stimuli; and
3 converting the instruction words to signals that, when applied to the bus,
4 execute at least one phase of a bus transaction.
- 1 22. The method of claim 21, further comprising the acts of:
2 defining a sequence of desired bus transactions; and
3 assembling the sequence of desired bus transactions into an object file
4 comprising instruction words representing predefined bus stimuli
5 that, when applied to a bus, implement the sequence of bus
6 transactions.

- 1 23. The method of claim 21, further comprising the act of providing
2 predefined signals to the bus in response to signals received from the bus.
- 1 24. The method of claim 21, further comprising the act of exchanging data
2 with agents on the bus.
- 1 25. A method for verifying the operation of at least one bus agent using a bus
2 transaction generator, the bus transaction generator providing bus stimuli
3 in response to a predefined sequence of bus transactions and in response to
4 signals received from the bus, the method comprising the acts of:
5 coupling at least one bus agent to the bus;
6 coupling the bus transaction generator to the bus;
7 defining the sequence of bus transactions;
8 assembling the sequence of bus transactions into an object file
9 representing bus stimuli;
10 initializing the at least one bus agent; and
11 executing the bus stimuli.
- 1 26. The method of claim 25, wherein the defining act includes bus stimuli that
2 when executed by the transaction generator, generates errors on the bus.
- 1 27. The method of claim 25, wherein the defining act comprises defining
2 processor-initiated bus transactions.
- 1 28. The method of claim 25, wherein at least one processor is coupled to the
2 bus, and wherein the defining act comprises defining bus transactions that
3 stimulate target agent bus transactions.